



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/759,267	01/20/2004	Geum-Jin Yun	2557-000206/US	6863
30593	7590	10/19/2005	EXAMINER	
HARNESS, DICKEY & PIERCE, P.L.C. P.O. BOX 8910 RESTON, VA 20195			PATEL, PARESH H	
			ART UNIT	PAPER NUMBER
			2829	

DATE MAILED: 10/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

21

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/759,267	YUN ET AL.	
	Examiner	Art Unit	
	Paresh Patel	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 29 August 2005.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1 and 3-29 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 27 is/are allowed.
- 6) ☒ Claim(s) 1,3-14,16-26,28 and 29 is/are rejected.
- 7) ☒ Claim(s) 15 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 January 2004 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>06/05</u>   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claims 1 and 3-29 have been considered but are moot in view of the new ground(s) of rejection.

### ***Drawings***

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference character "S15" in fig. 2A-B has been used to designate both "cooling" and "temperature control". Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.
3. Figure 3 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct

any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 3-14, 16-26 and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant disclosed prior art fig. 1-3 in view of Grosch et al. (US 6122760) and Eide (US 6014316).

Regarding claims 1, 7, 19 and 21, Applicant disclosed prior art (hereafter APA) in fig. 1-3 discloses a test method for testing a multi-chip package of multiple kinds of semiconductor devices (120, 122, 124) and testing the package with an integrated burn-in program (at least steps S10-S13 of fig. 2A and 2B). APA also discloses bin sorting at step S16 and contact test at step S11.

APA discloses all the elements as mentioned above except for the burn-in test program is adapted to test each of the semiconductor devices. However, APA discloses testing of each multi-chip package of multiple kinds of semiconductor devices, which requires additional burn-in board and three programs, one for each type of memory (fig. 3). It would have been obvious to a person having ordinary skill in the art at the time the

invention was made to test a multi-chip package of multiple kinds of semiconductor devices i.e. plurality of NAND FLASH MEMORY or plurality of SRAM or plurality of DRAM using test program of step S10 or S17 or S21 respectively (For example Fig. 7 of Eide reference (US 6014316) as TBGA, also see lines 16-39 of column 2 for testing), in order to test a multi-chip package of multiple kinds of semiconductor devices because same program test each of the semiconductor devices, to detect product failure rate, see fig. 1.

Regarding claims 3-4 and 16, APA discloses multiple kinds of semiconductor devices include one or more of non-volatile memory, SRAM, and DRAM (performs memory function).

Regarding claim 5, APA discloses test is conducted for each of the semiconductor devices at different temperature (at step S12, at step S12a etc.).

Regarding claim 6, APA discloses burn-in board and chamber as claimed before step S10.

Regarding claims 10, 22 and 24, APA discloses application of specific testing condition i.e. temperature, voltage and clock signal.

Regarding claims 11 and 25, APA discloses a single contact test at step S11.

Regarding claims 13 and 26, APA discloses a one time bin sorting at step S16.

Regarding claims 12 and 20, APA discloses monitoring burn-in test.

Regarding claims 8 and 14, APA discloses all the elements except for test program used a multiplexer selection function as claimed. Grosch et al. (hereafter Grosch) discloses a test program uses a multiplexer selection function as claimed. See

fig. 1 (16, 18 and 20), fig. 4 (18, 26 and 20) or fig. 6 where testing of both the devices 12 and 14, 14 and 34 or 10a and 10b are done simultaneously. Therefore. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify APA to include test program as claimed for simultaneous test of different kinds of semiconductor devices, in order to save testing time.

Regarding claims 9, 17 and 23, APA discloses all the elements except for test program have an I/O masking function for blocking some I/O terminals. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use test program as claimed to block I/O terminals, since test program with masking function as claimed is well known in the art for control application, particularly in code development program using address line.

Regarding claim 18, APA in fig. 3 discloses each semiconductor device has different number of I/O terminal pins.

Regarding claims 28-29, APA discloses loading the multi-chip package on the burn-in board and into a chamber as claimed before step S10.

### ***Allowable Subject Matter***

6. Claim 15 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. The following is a statement of reasons for the indication of allowable subject matter: No prior art has been found to meet the limitations of claim 15 calling for an

Art Unit: 2829

integrated burn-in test method for testing a multi-chip package comprising the burn-in test for each of the semiconductor devices is performed sequentially and the integrated burn-in test program controls the chamber temperature according to a test temperature for each of the semiconductor devices.

8. The following is an examiner's statement of reasons for allowance: No prior art has been found to meet the limitations of claim 27 calling for an integrated burn-in test method for testing a multi-chip package comprising testing each semiconductor devices of the multi-chip package with a test program including contact test and specific test condition as further defined at claim 27.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paresh Patel whose telephone number is 571-272-1968. The examiner can normally be reached on 8:00 to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nestor Ramirez can be reached on 571-272-2034. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Art Unit: 2829

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



October 16, 2005

Paresh Patel  
Primary Examiner  
Art Unit 2829